

VINITHA PASANHA

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PROFILE AND STRENGTHS

Backed by strong academic credentials: *M.Tech (VLSI Design and Embedded Systems), BE (Electronics and Communication)*; targeting assignments as *Faculty*; possess zeal to continue my teaching career at a highly-reputed and eminent educational institution and to gain exceptional career move ahead through long efforts and performance regularity.

- Perfect knowledge about the common job duties of a lecturer and ability to perform them efficiently
- Highly innovative in depicting the subject matter to the students/audience, using traditional methods as well as modern aids
- Ability to deal with complicated problems with my own tactics
- Dedication towards goal and work
- Posses excellent communication skills

EDUCATIONAL CREDENTIALS

Name of Institution	Course	Year	Result
1. NMAM Institute Of Technology, Nitte (Autonomous)	M.Tech	2013	85.4%
2.P.A College of Engineering, Mangalore(VTU)	B.E	2010	70.86%
3.St Aloysius College, Mangalore	P.U.C	2006	82.16%
4. St Ann's High School, Mangalore	S.S.LC	2004	89.28%

SOFTWARE PROFICIENCY AND TECHNICAL SKILLS

Language	Verilog, 8051 Microcontroller, VHDL
Tools	Cadence, Xilinx Vivado, Keil, Microwind, Microcap

WORK EXPERIENCE

1. ORGANISATION: St Joseph Engineering College, Vamanjoor

Duration: February 2017 – June 2020 (3 years)

Position Held: Assistant Professor

Subjects Handled: Basic Electronics, Verilog HDL, HDL lab, VLSI Design, Embedded Systems(M.Tech).

2. ORGANISATION: Young Scholars Academy, Bangalore

Duration: May 2016 – January 2017

Position Held: Facilitator

Subjects Handled: Computer Science, Maths

3. ORGANISATION: National Institute of Technology, Suratkal

Duration: July 2014 – November 2014 (5 months)

Position Held: Assistant Lecturer

Subjects Handled: Elements of Electronics and Communication engineering, Digital Electronics Laboratory.

4. ORGANISATION: Shree Devi Institute of Technology, Mangalore

Duration: August 2013 – December 2013 (4 months)

Position Held: Assistant Professor

Subjects Handled: Computer Communication Networks, CMOS VLSI Design (M.Tech) and Analog Electronics Circuits Laboratory.

5. ORGANISATION: DARE, DRDO, Bangalore

Duration: August 2012-April 2013 (9 months)

Position Held: Intern (Hardware Division)

Responsibilities: Circuit Design, Circuit Schematic, Pre-layout Signal Integrity Analysis.

6. ORGANISATION: MVSIT, Moodabidri

Position Held: Lecturer.

Duration: August 2010- September 2011 (13 months).

Subjects Handled: Fundamentals of CMOS VLSI, Analog and Mixed mode VLSI, Basic Electronics.

ACADEMIC PROJECT

Engineering Project

Real time ECG machine with data transmission through GSM

Description: This project describes a low-cost, portable system with wireless transmission capabilities for the acquisition, processing, storing and visualization in real time of the electrical activity of the heart to a mobile phone or PC.

M.Tech Project

Fibre optic based mezzanine module design for video transfer using ARINC 818 protocol (Hardware Design)

Organisation: DARE, DRDO, Ministry of defence

Description: Being a part of the hardware design team, my main task was performing signal integrity analysis on the various components selected, in order to overcome crosstalk, Electromagnetic interference and signal integrity issues. I was responsible for library creation for the various components and also some part of schematics using OrCad tool.

ACHIEVEMENT

Published a paper titled “Signal Integrity analysis of High Speed devices” in the International Journal/ Conference of Enhanced Research in Science, Technology and Engineering (IJERSTE) in Volume 2, Issue 4, April 2013. (ISSN No:2319-7463)

Part of the organizing committee in the **National Conference NCACSP-2017**

Successfully completed NPTEL Online Certification course on **CMOS Digital VLSI Design** with a consolidated score of 51%

Successfully completed NPTEL Online Certification course on **Digital Circuits** with a consolidated score of 61%

Successfully completed NPTEL Online Certification course on **Microprocessors and Microcontrollers** with a consolidated score of 56%

WORKSHOPS ATTENDED

Three days workshop on “**Advanced Digital System Design and Verification using Xilinx Vivado and Cadence Design Suite**”

Three days FDP on “**Research Opportunities in Bio-Medical Engineering**”

Five days FDP on “**Embedded Systems for Communication Applications**”

“**FEEL TEACHER**” Learning and Development Intervention by CLHRD

FDP on “**New age skills for excellence in teaching**”

Four days FDP on “**FINFET based VLSI Design using Cadence**”

Three days FDP on “**Research Opportunities in Bio-Medical Engineering**”

Two day workshop on “**ARM Cortex M3 Embedded Controller**”

PERSONALITY TRAITS

- Can work efficiently in a group as well as an individual and take up responsibilities
- Confidence in my effort and hard work, keen to know more
- Good leadership qualities and communication skills
- Flexible and understanding
- Moral values

PERSONAL DETAILS

Name : Vinitha Pasanha
Gender : Female
Marital status : Married
DOB : 19 December 1987
Languages Known : English, Kannada, Konkani, Hindi

DECLARATION

I hereby declare that all the information stated above is true up to my knowledge.

Place: Mangaluru

Date: 25 June 2024

(Vinitha Pasanha)